WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory blocks each having a plurality of memory cells arranged in rows and columns;

a plurality of sense amplifier bands arranged in correspondence to said plurality of memory blocks so as to be shared between adjacent memory blocks, each sense amplifier band including a plurality of sense amplifiers each sensing and amplifying data in a memory cell in a corresponding memory block when activated;

a plurality of bit line isolation circuits, arranged in correspondence to said plurality of sense amplifier bands, for electrically connecting, when made conductive, corresponding sense amplifier bands to corresponding memory blocks; and

a bit line isolation control circuit for setting at least the bit line isolation circuit provided for a specific memory block to be nonconductive in a standby mode of operation.

2. The semiconductor memory device according to claim 1, wherein

said bit line isolation control circuit maintains said plurality of bit line isolation circuits to be nonconductive in said standby mode of operation, to isolate said plurality of memory blocks from the corresponding sense amplifier bands.

3. The semiconductor memory device according to claim 1, wherein

said bit line isolation control circuit includes a program circuit generating a signal for specifying said specific memory block, and the memory blocks other than said specific memory block are electrically connected to the corresponding sense amplifier bands through the corresponding bit line isolation circuits in said standby mode of operation.

4. The semiconductor memory device according to claim 1, wherein

said semiconductor memory device has a normal operation mode for

making data access and a data holding mode for holding data stored in the memory cells, and

said bit line isolation control circuit sets said plurality of bit line isolation circuits to be nonconductive at a standby state during activation of a refresh mode instruction signal designating said data holding mode.

5. The semiconductor memory device according to claim 4, wherein said bit line isolation control circuit controls the bit line isolation circuits so as to electrically connect said plurality of memory blocks to the corresponding sense amplifier bands at said standby state when said data holding mode instruction signal is deactivated.

6. The semiconductor memory device according to claim 1, wherein said bit line isolation control circuit includes

a plurality of bit line isolation select control circuits, arranged in correspondence to said bit line isolation circuits, each for selecting one of a first bit line isolation control signal generated on the basis of a first memory block select signal specifying the memory block arranged for a corresponding bit line isolation circuit and a second bit line isolation control signal generated on the basis of a second memory block select signal specifying the memory block sharing the corresponding sense amplifier band in accordance with a mode selection signal, to apply a selected one to the corresponding bit line isolation circuit as a isolation control signal, said first bit line isolation control signal and said second bit line isolation control signal being opposite in logic to each other.

7. The semiconductor memory device according to claim 6, wherein each of said bit line isolation control circuits selects said second bit line isolation control signal in accordance with said mode selection signal in a data holding mode for holding data of the memory cells, said second isolation control signal being equal in logic level to said isolation control signal when selected.

8. The semiconductor memory device according to claim 6, wherein said mode selection signal is an operation mode designation signal designating a data holding mode.

9. The semiconductor memory device according to claim 6, wherein said mode selection signal is a combined signal of an isolation select activation signal set for each memory block and a mode instruction signal designating a data holding mode, and is programmed for each of said plurality of memory blocks.

10. The semiconductor memory device according to claim 6, wherein said mode selection signal is generated for each memory block by a program circuit arranged for each of said plurality of memory blocks.